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10/677,629	10/02/2003	Kah-Ho Phong	851663.455	4188

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EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/677,629	**Applicant(s)** PHONG ET AL.
	Examiner Joni Hsu	**Art Unit** 2676

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-15* is/are rejected.
7)☒ Claim(s) *14* is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☒ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

> It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract is 152 words in length and therefore exceeds 150 words.

3. The disclosure is objected to because of the following informalities: According to MPEP § 608.01 (m), the present Office practice is to insist that each claim must be the object of a sentence starting with "I (or we) claim," "The invention claimed is" (or the equivalent). The

phrase "Claims" is not considered equivalent to these appropriate phrases. Appropriate correction is required.

Claim Objections

4. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

There are two claims that are numbered 14. The second misnumbered claim 14 has been renumbered 15.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-4, 6, 7, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herluison (US005696698A) in view of Zhang (US20010050955A1), further in view of Cook (US 20020101536A1).

8. With regard to Claim 1, Herluison describes a cache memory system for use in a motion estimation system (Col. 1, lines 8-13), comprising: a first cache memory (2, Figure 1) defined in terms of a first width (m) and a first height (n) (Col. 4, lines 17-19), and a second cache memory (1) defined in terms of a second width (m/2) and a second height (n), wherein the second width is less than the first width (Col. 4, lines 28-32); an arrangement having banks of memory from the second cache memory concatenated horizontally (Col. 4, lines 45-49) such that their concatenated width is at least equal to the first width (Col. 4, lines 10-39), as shown in Figure 1. Figure 1 shows that the banks of memory from the first and second caches are stacked horizontally, but Herluison describes that they are also stacked vertically (Col. 4, lines 45-49). If they are stacked vertically, then the width becomes the height and the height becomes the width. In that case, the second height is less than the first height. Since the banks are also stacked vertically, Herluison describes an arrangement having banks of memory from the first and second caches stacked vertically, and arranged to be addressed as two separate address spaces (Col. 3, lines 17-27).

However, Herluison does not teach that the banks of memory from the first and second caches are stacked together vertically. However, Zhang describes a motion estimation system [0033, 0081] that searches a cache memory (402, Figure 11) with all the banks of memory concatenated vertically or stacked together vertically [0131].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Herluison so that the banks of memory from the first and second caches are stacked together vertically as suggested by Zhang because Zhang suggests that accessing vertical caches together optimizes the speed [0077].

However, Herluison and Zhang do not teach that in the first arrangement, the concatenated banks of the second cache memory are arranged to be appended to the width of the first cache memory to form a single contiguous address space. However, Cook describes a motion estimation system [0028] with a cache memory arrangement having banks of memory from the second cache memory (UV, chrominance) concatenated horizontally such that their concatenated width is at least equal to the first width, and the concatenated banks being arranged to be appended to the height of the first cache memory (Y, luminance) to form a single contiguous address space [0039], as shown in Figure 3B. However, Herluison described that the banks are also concatenated vertically. Therefore, combining Herluison and Zhang, if the banks of Zhang were concatenated vertically instead of horizontally, the concatenated banks of the second cache memory would arranged to be appended to the width of the first cache memory instead of the height to form a single contiguous address space.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Herluison and Zhang so that in the first arrangement, the concatenated banks of the second cache memory are arranged to be appended to the width of the first cache memory to form a single contiguous address space as suggested by Cook. Cook suggests that this format (planar YUV 4:2:0) is the digital component format used to perform MPEG-2 motion compensation, and this is well-known in the art and widely used [0024].

9. With regard to Claim 2, Herluison describes that the first and second heights are equal (n, Figure 1; Col. 4, lines 17-19, 27-32). As discussed in the rejection for Claim 1, if the banks are stacked vertically, then the width becomes the height and the height becomes the width. Therefore, when stacked vertically, the first and second widths are equal.

10. With regard to Claim 3, Herluison does not teach that the first arrangement is for use with a motion estimation system having a single search area. However, Cook describes a motion estimation system [0028] having a single search area (Figure 3B) [0039], as discussed in the rejection for Claim 1.

11. With regard to Claim 4, Herluison describes that the second arrangement is for use with a motion estimation system having two separate search areas (1, 2, Figure 1; Col. 3, lines 18-27; Col. 4, lines 10-39).

12. With regard to Claim 6, Claim 6 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

13. With regard to Claim 7, Herluison does not teach that the motion estimation system is operable according an MPEG standard. However, Cook describes teach that the motion estimation system is operable according an MPEG standard [0028].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Herluison so that the motion estimation system is operable according an MPEG standard as suggested by Cook because Cook suggests that operating according an MPEG standard such as an MPEG-2 standard is well-known in the art and widely used [0020].

14. With regard to Claim 10, Claim 10 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

15. With regard to Claim 11, Claim 11 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

16. With regard to Claim 12, Herluison describes using the first arrangement as a single logical cache in the motion estimation system (Col. 1, lines 8-13) by simultaneously searching in the first (s1, s2, Figure 1) and second banks (s3, s4) of the second cache memory (1) as a single search area (Col. 4, lines 10-39).

17. Claims 5, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herluison (US005696698A) in view of Zhang (US20010050955A1), further in view of Cook (US 20020101536A1), further in view of Chen (US005535288A).

18. With regard to Claim 5, Herluison, Zhang, and Cook are relied upon for the teachings as discussed above relative to Claim 4.

However, Herluison, Zhang, and Cook do not teach that the two separate search areas are of equal size. However, Chen describes a motion estimation system (Col. 1, lines 12-17) with two separate search areas (59, 61, Figure 4; Col. 6, lines 62-67). Figure 5 shows the relative size of the search block, showing search block 59 as an example (Col. 5, lines 42-43; Col. 7, lines 7-45). Chen describes that typically, the search block is restricted to 32x32 pixels (Col. 2, lines 19-21). Therefore, the two separate search areas are inherently of equal size.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Herluison, Zhang, and Cook so that the two separate search areas are of equal size as suggested by Chen. Chen suggests that it is advantageous for the two separate search areas to be of equal size and restricted to a certain size to make it easier to find a "best match" (Col. 2, lines 6-30).

19. With regard to Claim 13, Herluison does not teach using the second arrangement as first and second logical caches in the motion estimation system by searching in the memory banks of only the first cache memory as the first logical cache and searching in the memory banks of the second cache memory and in a portion of the memory banks of the first cache memory as the

second logical cache. However, Chen describes a motion estimation system (Col. 1, lines 11-17) that searches in the memory banks of only the first cache memory as the first logical cache (Method B 101, Figure 7) and searching in the memory banks of the second cache memory and in a portion of the memory banks of the first cache memory as the second logical cache (Method A 100, Figure 6; Col. 7, lines 55-63).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Herluison, Zhang, and Cook to include using the second arrangement as first and second logical caches in the motion estimation system by searching in the memory banks of only the first cache memory as the first logical cache and searching in the memory banks of the second cache memory and in a portion of the memory banks of the first cache memory as the second logical cache as suggested by Chen because Chen suggests that the first logical cache (Method B 101) requires less cache memory and the second logical cache (Method A 100) contains more repetitions of elementary subroutines, and both are advantageous for certain situations (Col. 7, lines 55-63).

20. With regard to Claim 14, Herluison, Zhang, and Cook do not teach the method of Claim 13 wherein the searching steps are performed simultaneously. However, Chen describes the method of Claim 13 as discussed above, wherein the searching steps are performed simultaneously (Col. 7, lines 55-63).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Herluison, Zhang, and Cook to include the method of Claim 13 wherein the searching steps are performed simultaneously as suggested by Chen because

Chen suggests that performing the searching simultaneously increases the speed of the search (Col. 4, lines 36-42).

21. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herluison (US005696698A) in view of Zhang (US20010050955A1), further in view of Cook (US 20020101536A1), further in view of Kopet (US005510857A).

Herluison, Zhang, and Cook are relied upon for the teachings as discussed above relative to Claim 6.

However, Herluison, Zhang, and Cook do not teach that the cache memory system is arranged to be addressed as a circular buffer. However, Kopet describes a motion estimation system (Col. 2, lines 51-53) with a memory system arranged to be addressed as a circular buffer (Col. 20, lines 4-9).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Herluison, Zhang, and Cook so that the cache memory system is arranged to be addressed as a circular buffer as suggested by Kopet. Circular buffers well-known in the art and widely used. Circular buffers automatically generate and increment pointers for memory accesses which wrap to the beginning of the buffer when its end is reached, thus saving the time and instructions otherwise needed to ensure that the address pointer stays within the boundary of the buffer, and speeding the executing of repetitive DSP algorithms. These advantages of circular buffers can be found in many publications, such as the hyperdictionary website.

22. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herluison (US005696698A) in view of Zhang (US20010050955A1), further in view of Cook (US 20020101536A1), further in view of Dye (US006567091B2).

Herluison, Zhang, and Cook are relied upon for the teachings as discussed above relative to Claim 6.

However, Herluison, Zhang, and Cook do not teach that the motion estimation system includes means for addressing the cache memory system including a start pointer for indicating the start of a search area; an update pointer for indicating a bank being updated; and a search width parameter for indicating the extent of the search area. However, Dye describes that the motion estimation system (Col. 76, lines 60-67) includes means for addressing the cache memory system (838, Figure 33; Col. 70, line 38-Col. 71, line 16; Col. 74, lines 1-13) including a start pointer for indicating the start of a search area and an update pointer for indicating a bank being updated (Col. 78, lines 19-49). Dye also describes that the device knows when a buffer is filled with data from video frames for motion estimation, which is the search area (Col. 77, lines 21-37). Therefore, there must inherently be a search width parameter for indicating the extent of the search area.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Herluison, Zhang, and Cook so that the motion estimation system includes means for addressing the cache memory system including a start pointer for indicating the start of a search area; an update pointer for indicating a bank being updated; and a search width parameter for indicating the extent of the search area as suggested by Dye. Dye suggests that using these pointers is advantageous because the graphics data need not be stored in contiguous memory locations as with a traditional frame buffer (Col. 2, lines 40-47). Dye also describes that it is not required to maintain a single frame buffer which contains all of the video data for display on the video screen. Rather the video data for the various windows and objects is stored in respective memory areas in the system memory, and pointers assembled are used to reference this data during screen updates. Thus, data is not required to be moved in or out of a frame buffer to reflect screen changes, but rather in many instances either the video data for a respective window or object is changed, or only the pointers are manipulated (Col. 6, lines 1-17). It also would have been obvious to have a search width parameter for indicating the extent of the search area so that the device knows when a buffer is filled with data from video frames for motion estimation, which is the search area (Col. 77, lines 21-37).

23. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herluison (US005696698A) in view of Zhang (US20010050955A1), further in view of Cook (US 20020101536A1), further in view of Chen (US005535288A), further in view of Corset (US005995668A).

Herluison, Zhang, Cook, and Chen are relied upon for the teachings as discussed above relative to Claim 13.

However, Herluison, Zhang, Cook, and Chen do not teach that searching in the first logical cache includes searching for forward/backward motion of a video sequence and searching in the second logical cache includes searching for foreground/background motion of the video sequence. However, Corset describes a motion estimation circuit and a motion compensation circuit (Col. 3, lines 24-25). The motion estimation circuit searches for foreground/background motion of the video sequence (Col. 14, lines 12-36). The motion compensation circuit searches for forward/backward motion of a video sequence (Col. 14, lines 1-11).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Herluison, Zhang, Cook, and Chen so that searching in the first logical cache includes searching for forward/backward motion of a video sequence and searching in the second logical cache includes searching for foreground/background motion of the video sequence as suggested by Corset. Corset suggests that searching for forward/backward motion of a video sequence is necessary for motion compensation. As the motion vectors start from an integer pixel location but point to a non-integer one, the locations of the pixels of the current reconstructed partition have to be quantized in the forward case, where as in the backward case, the locations of the pixels of the previously reconstructed partition are quantized (Col. 14, lines 1-11). Corset also suggests that searching for foreground/background motion of the video sequence is necessary for motion estimation. A distinction has to be made between the motion of the pixels inside a region (texture motion) and the motion of its shape. Both motions coincide in the case of a rigid foreground region, but not for a background region because the modifications of its shape or of its contours are defined by the motion of the regions in its foreground. The motion estimation for contours is replaced by an extra information called order relation between regions and which allows to know for every couple of neighboring regions which of them is on the foreground, and this order information is associated to the texture motion in order to compensate both the partition and the texture (Col. 14, lines 12-36).

Prior Art of Record

"Hardware Circular Buffer",

http://www.hyperdictionary.com/computing/hardware+circular+buffer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 703-305-4418. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Matthew C. Bella

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